EAST - [10766902 trench dram with test structure.wsp:1]

File View Edit Tools Window Help

L15: (70) 14 near 7
L16: (1) 10 with 15
L17: (18229) 11 near9 8
L18: (23559) 11 with 8
L19: (711178) transistor tft
L20: (1858996) vertical
L21: (16301) 19 near2 (20 14)
L22: (19773) 19 near2 (20 14 11)
L23: (231) 22 same 10
L24: (3442) 10 near12 8
L25: (5) 24 same 22
L26: (5) 24 same 23
L27: (3) "6617180".pn.
L28: (97116) dram
L29: (601739) capacitor
L30: (6155) 11 near 29
L31: (54) 10 with 30
L32: (37) 31 and (28 22)
L33: (89) 7 with 10
L34: (2755052) leakage capacitance characteristic
L35: (1) 33 with 34
L36: (5) 33 same 34
L37: (1629260) (transfer)
L38: (288) 37 near 7
L39: (1) 38 with 10
Failed

Browse Clear

DBs US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB Plurals

Default operator: OR Highlight all hit terms initially

24 same 23

Rec - 2004

BRS form ISR form Image Text HTML

	U	S	Inventor	Document	Issue	P	Title	Current	CurrentXR	Retrieval	S	C	P				Image Doc.	P
1			Wang, Jianguo et al.	US 200402080 55 A1	20041 021	3 0	Methods and circuits for testing programmability of a semiconductor memory cell and memory array using a breakdown ph	365/182									US 200402080 55	
2			Pio; Federico et al.	US 6128219 A	20001 003	2 3	Nonvolatile memory test structure and nonvolatile memory reliability test method	365/185 .09	365/185.05 ; 365/185.24								US 6128219	
3			Kowalski, Bernhard et al	US 200402455 89 A1	20041 209	1 0	Device architecture and process for improved vertical memory arrays	257/328									US 200402455 89	
4			Tomita; Naoto et al.	US 5432745 A	19950 711	2 0	Method for testing a memory device	365/201	365/200								US 5432745	

Hits Details HTML

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